REMARKS

Claims 24-35 are pending in the present patent application. Claims 25-27 and 31-33 are allowed. Claims 24, 28-30, 34, and 35 stand rejected. This application continues to include claims 24-35.

Applicant thanks the Examiner for allowing claims 25-27 and 31-33.

Claims 24, 28-30, 34, and 35 were rejected as being anticipated by Potucek, et al., U.S. Patent No. 5,253,934 (hereinafter, Potucek). Applicant respectfully requests reconsideration of the rejection of claims 24, 28-30, 34, and 35 in view of the following.

Potucek is directed to circuitry on a printer for controlling signals flowing to a printhead forming part of the printer apparatus to control current uniformity to the recording elements (col. 1, lines 32-35). Potucek discloses a linear array 10 of 3584 triggerable recording elements (LEDs), disposed to expose selectively a photosensitive image-receiver medium 12 that is movable relative to the array (col. 3, lines 20-25). Associated with each LED is a data register means 24 for latching data from a bus during each cycle of operation for printing a single line of dots or pixels (col. 6, lines 13-16). A token bit is used to enable the data register means associated with a particular LED to accept the data while other data register means associated with other LED's await their respective data (col. 6, lines 17-20).

Buffers 31 with enable inputs and direction controls are coupled to a token bit shift register 28 so that programmable control may be made of the direction for shifting the token bit along the token bit shift register 28 (col. 6, lines 45-50). In the example where the token bit is to be shifted from left to right in FIG. 4 for the Data Odd half of the printhead, the signal line TDIR

(token direction) is made at an appropriate logic level to allow the token bit on line LTOKEN to pass from left to right (col. 6, lines 50-54). Thus, in response to clock pulses from the data processor 16 the token bit is passed from stage to stage (left to right in FIG. 4) of the token bit shift register 28 and accordingly outputted sequentially over respective lines 21 through OR gates 11 to lines 27 for enablement of all the master latches 25 of a respective data register 24 (col. 6, lines 54-60). With movement of the token bit from stage to stage of the shift register 28, the data bits occurring on lines DI0-DI5 are accepted by the data registers 24 in turn from left to right until all the 1792 data registers on this side of the printhead have acquired their respective six bits of data (col. 6, lines 60-65).

Applicant believes that claims 24, 28-30, 34, and 35 patentably define Applicant's invention over Potucek, for at least the reasons set forth below.

Claim 24 is directed to a supply item comprising a circuit including a tri-state input port, said supply item associated with an imaging apparatus, and said supply item having at least three modes of operation, wherein a particular mode of operation of said at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to said tri-state input port.

Potucek does not disclose, teach, or suggest a supply item having a circuit including a tri-state input port, as recited in claim 24, much less wherein the supply item has at least three modes of operation, wherein a particular mode of operation of the at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to the tri-state input port, as recited in claim 24.

In contrast to claim 24, Potucek discloses triggerable recording elements in the form of LEDs (col. 3, lines 20-25), wherein associated with each LED is a data register means 24 for latching data from the bus during each cycle of operation for printing a single line of dots or pixels (col. 6, lines 13-16). In order to latch data, a token bit is used to enable the data register means associated with a particular LED to accept the data while other data register means associated with other LED's await their respective data (col. 6, lines 17-20). Potucek discloses that buffers 31 with enable inputs and direction controls are coupled to a token bit shift register 28 so that programmable control may be made of the direction for shifting the token bit along the token bit shift register 28 (col. 6, lines 45-50).

However, Potucek does not disclose, teach, or suggest that the buffers 31 have or include tri-state input ports, and does not disclose, teach, or suggest wherein a particular mode of operation of at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to a tri-state input port.

Rather, Potucek simply discloses that where the token bit is to be shifted from left to right in FIG. 4 for the Data Odd half of the printhead, the signal line TDIR (token direction) is made at an appropriate logic level to allow the token bit on line LTOKEN to pass from left to right (col. 6, lines 50-54), and that thus, in response to clock pulses from the data processor 16, the token bit is passed from stage to stage (left to right in FIG. 4) of the token bit shift register 28 and accordingly outputted sequentially over respective lines 21 through OR gates 11 to lines 27 for enablement of all the master latches 25 of a respective data register 24 (col. 6, lines 54-60).

Thus, Potucek discloses that that the logic value in signal line TDIR governs the direction that the token bit from the LTOKEN line is passed, but does not disclose, teach, or suggest that

the token bit or the logic level of the TDIR signal line have three different values such as might otherwise represent a tri-state signal, much less that the electronic components that receive such signals have tri-state input ports.

Although the Examiner asserts that the Potucek TDIR (Fig. 4A) is a tri-state input port of the Potuck buffer 31, Applicant respectfully submits that Potucek does not in any way disclose, teach, or suggest that the TDIR signal line transmits a tri-state signal, or that the buffer 31 is capable of receiving and operating upon a tri-state signal. Rather, the TDIR signal line is for determining whether the token bit will be passed from left to right or right to left, which pertains to two possible states, not three, such as might otherwise disclose, teach, or suggest a tri-state signal.

In addition, Potucek Fig. 9 discloses that there are two TDIR bit values: TDIR = 0, which directs the token bit to "GO TOWARD LEFT," and TDIR = 1, which directs the token bit to "GO TOWARD RIGHT." Thus, Potucek discloses that the TDIR signal line transmits a two-state signal to buffer 31, not a tri-state signal.

Accordingly, Potucek does not disclose, teach, or suggest a supply item comprising a circuit including a tri-state input port, the supply item associated with an imaging apparatus, and the supply item having at least three modes of operation, wherein a particular mode of operation of the at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to the tri-state input port, as recited in claim 24.

Accordingly, for at least the reasons set forth above, Applicant believes that 24 is in condition for allowance in its present form.

Claims 28 and 29 are believed allowable due to their dependence, directly or indirectly, on otherwise allowable base claim 24. In addition, claims 28 and 29 further and patentably define the invention over Potucek.

Claim 30 is directed to an imaging apparatus. Claim 30 recites, a controller; and a supply item for use in said imaging apparatus including a circuit having a tri-state input port coupled to said controller, said supply item having at least three modes of operation, wherein a particular mode of operation of said at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to said tri-state input port by said controller.

Potucek does not disclose, teach, or suggest a tri-state input port coupled to the Potucek logic and control device (LCU) 13, but rather, discloses that the asserted tri-state input port, which is the Potucek TDIR signal line, is coupled to a data processor 16 in the form of a raster image processor. For example, Figs. 2-4 depict that the Potucek driver circuits 40 receive data, including the token bit, from RIP 16 of Fig. 2.

The RIP device of Fig. 2, identified with reference character "16," is a raster image processor (col. 3, lines 49-53), which is not a "controller" within the context of Applicant's claimed invention.

Although Potucek discloses a logic and control device (LCU) 13, Potucek does not disclose, teach, or suggest any connections as between LCU 13 and a circuit having a tri-state input port such as might otherwise disclose, teach, or suggest a circuit having a tri-state input port coupled to a controller, as recited in claim 30 (Fig. 2).

While the Examiner asserts that the "circuit connected to 31" is a controller, Applicant respectfully submits that Potucek discloses that the asserted circuit is a driver circuit (col. 2, lines 56-58), which is not a controller within the context of Applicants' claimed invention.

In addition, in contrast to the supply item having at least three modes of operation, wherein a particular mode of operation of the at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to the tri-state input port by the controller, as recited in claim 30, Potucek discloses triggerable recording elements in the form of LEDs (col. 3, lines 20-25), wherein associated with each LED is a data register means 24 for latching data from bus during each cycle of operation for printing a single line of dots or pixels (col. 6, lines 13-16).

In order to latch data, a token bit is used to enable the data register means associated with a particular LED to accept the data while other data register means associated with other LED's await their respective data (col. 6, lines 17-20). Potucek discloses that buffers 31 with enable inputs and direction controls are coupled to a token bit shift register 28 so that programmable control may be made of the direction for shifting the token bit along the token bit shift register 28 (col. 6, lines 45-50).

However, Potucek does not disclose, teach, or suggest that the buffers 31 have or include tri-state input ports, and does not disclose, teach, or suggest wherein a particular mode of operation of the at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to the tri-state input port by the controller.

Rather, Potucek simply discloses that where the token bit is to be shifted from left to right in FIG. 4 for the Data Odd half of the printhead, the signal line TDIR (token direction) is made at

an appropriate logic level to allow the token bit on line LTOKEN to pass from left to right (col. 6, lines 50-54), and that thus, in response to clock pulses from the data processor 16, the token bit is passed from stage to stage (left to right in FIG. 4) of the token bit shift register 28 and accordingly outputted sequentially over respective lines 21 through OR gates 11 to lines 27 for enablement of all the master latches 25 of a respective data register 24 (col. 6, lines 54-60).

Thus, Potucek discloses that that the logic value in signal line TDIR governs the direction that the token bit from the LTOKEN line is passed, but does not disclose, teach, or suggest that the token bit or the logic level of the TDIR signal line have three different values such as might otherwise represent a tri-state signal, much less that the electronic components that receive such signals have tri-state input ports.

Although the Examiner asserts that the Potucek TDIR (Fig. 4A) is a tri-state input port of the Potuck buffer 31, Applicant respectfully submits that Potucek does not in any way disclose, teach, or suggest that the TDIR signal line transmits a tri-state signal, or that the buffer 31 is capable of receiving and operating upon a tri-state signal. Rather, the TDIR signal line is for determining whether the token bit will be passed from left to right or right to left, which pertains to two possible states, not three, such as might otherwise disclose, teach, or suggest a tri-state signal.

In addition, Potucek Fig. 9 discloses that there are two TDIR bit values: TDIR = 0, which directs the token bit to "GO TOWARD LEFT," and TDIR = 1, which directs the token bit to "GO TOWARD RIGHT." Thus, Potucek discloses that the TDIR signal line transmits a two-state signal to buffer 31, not a tri-state signal.

Accordingly, Potucek does not disclose, teach, or suggest a supply item for use in the imaging apparatus including a circuit having a tri-state input port coupled to the controller, the supply item having at least three modes of operation, wherein a particular mode of operation of the at least three modes of operation is selected based on a signal level of a tri-state input signal supplied to the tri-state input port by the controller, as recited in claim 30.

Claims 34 and 35 are believed allowable due to their dependence, directly or indirectly, on otherwise allowable base claim 30. In addition, claims 34 and 35 further and patentably define the invention over Potucek.

Accordingly, for at least the reasons set forth above, Applicant believes that claims 24, 28-30, 34, and 35 are in condition for allowance in their present respective forms, and thus respectfully requests that the rejection of claims 24, 28-30, 34, and 35 under 35 U.S.C. 102(b) be withdrawn.

For the foregoing reasons, Applicant submits that no combination of the cited references teaches, discloses or suggests the subject matter of the appended claims. The appended claims are therefore in condition for allowance, and Applicant respectfully requests withdrawal of all rejections and allowance of the claims.

In the event Applicant has overlooked the need for an extension of time, an additional extension of time, payment of fee, or additional payment of fee, Applicant hereby conditionally petitions therefor and authorizes that any charges be made to Deposit Account No. 20-0095, TAYLOR & AUST, P.C.

Should any question concerning any of the foregoing arise, the Examiner is invited to telephone the undersigned at (317) 894-0801.

Respectfully submitted,

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